

# JASON J. NEMETH

Cincinnati, Ohio • Write to [jason@jason-nemeth.com](mailto:jason@jason-nemeth.com) for full contact information

## SUMMARY

---

Experienced digital design engineer and technical team lead with an outstanding record of success in driving programs throughout all phases of their life cycle, including proposal development, requirement and specification definition, implementation, verification, and maintenance. Demonstrates a strong commitment to producing quality products through effective leadership and a meticulous attention to detail. Combines exemplary communication and technical skills with extensive experience developing and implementing wireless FPGA-based digital signal processing systems for Software Defined Radios (SDRs) and Intellectual Property (IP) cores to deliver products within time and budget constraints.

## TECHNICAL SKILLS

---

**TOOLS:** Mentor Graphics ModelSim, Synopsys Synplify, Xilinx ISE, Altera Quartus II, Subversion, Texas Instruments Code Composer Studio, Microsemi (Actel) Libero, Simics, Xcode

**LANGUAGES:** VHDL, MATLAB, C++, C, Objective-C, Python, Verilog, Java, Ruby, OpenGL

**MISCELLANEOUS:** CMMI, SCAMPI Appraisals, iPhone & iPod Application Development

## PROFESSIONAL EXPERIENCE

---

L-3 COMMUNICATIONS NOVA ENGINEERING February 2008 – Present

Senior Digital Design Engineer (March 2011 – Present)

- Led a multi-disciplinary team of seven engineers in implementing and validating a low resource utilization and low data rate transceiver from the ETSI DVB-S2 Specification, a European digital satellite-based television broadcasting standard. Performed proposal and bidding, assisted in planning and developing system architecture, led implementation team including developing VHDL and bit-true MATLAB models, and validated system using commercial tools to ensure compliance with the standard.
- Created and tested Mobile DDR interfacing and control components to assist in porting the Wideband Networking Waveform (WNW) to a new SDR platform by reducing RAM utilization within the FPGA.
- Performed a full CMMI SCAMPI appraisal suite that resulted in the company being officially rated by the Carnegie Mellon Software Engineering Institute (SEI) at Maturity Level 3.

Digital Design Engineer (June 2009 – March 2011)

- Led a team of four engineers through planning, implementation, and qualification testing of the SpeedNet Euro four channel 16PSK MANET Smart Grid radio capable of closing links of over four miles using a one watt power amplifier (PA). Performed proposal and bidding, planned and developed system architecture, led implementation team, and validated against system and Conformité Européenne (CE) mark requirements.
- Developed a WiMAX-compatible LDPC FEC Encoder core capable of achieving over 40 Mbps while maintaining requirements for low FPGA resource utilization across several different vendors and families.
- Implemented digital up conversion (DUC) and digital down conversion (DDC) components to allow a custom OFDM-based waveform to work at multiple clock rates while maintaining spectral mask requirements at intermediate frequency (IF), radio frequency (RF), and PA outputs.
- Worked directly with customers to develop and refine new business proposals based upon their needs while simultaneously reviewing prior similar projects to agree upon feasible schedule and budgetary milestones.

Associate Digital Design Engineer (February 2008 – June 2009)

- Designed, implemented, and performed qualification testing for the All-Terrain Data Link (ATDL), a WNW OFDM-based radio capable of transmitting an HD video feed from an automated terrestrial reconnaissance vehicle at the US Army's Aberdeen Proving Ground.

Continued on the following page

- Created process documents and coding standards aimed at producing components and code at a consistently high quality level, and set up tools to monitor the effectiveness of these processes.
- Researched and provided recommendations for the hardware and software components to be used for a company-wide standard radio development platform.

**GENERAL ELECTRIC AVIATION**

September 2002 – April 2006

## Computer Engineering Co-Op

- Created MateCheck software as a cost-effective PC-based replacement for expensive proprietary turbine engine balancing machines by developing the hardware interfaces and software algorithms to pinpoint and resolve sources of imbalance within the engine rotor assemblies. Traveled to engine assembly facilities to teach assembly workers about the new balancing process and to assist with its implementation at the plants.
- Designed and implemented software to convert engine performance data into Air Force Technical Orders, reducing processing time from approximately six hours to only a few minutes per report.

**EDUCATION**

## UNIVERSITY OF CINCINNATI – Cincinnati, Ohio

September 2005 – June 2008

Master of Science in Computer Engineering – GPA: 3.8/4.0

- Very Large Scale Integration (VLSI) Research Group
- Thesis work involved development, modeling, and simulation of an advanced microprocessor cache design capable of reducing both access latency and power consumption in single-chip multiprocessors.

## UNIVERSITY OF CINCINNATI – Cincinnati, Ohio

September 2000 – June 2005

Bachelor of Science in Computer Engineering – GPA: 3.3/4.0

- Minor in VLSI Design and Analysis
- Minor in Mathematics

**PUBLICATIONS**

## IEEE TRANSACTIONS ON VLSI SYSTEMS

January 2011

“Location Cache Design and Performance Analysis for Chip Multiprocessors” (Volume 19, Pages 104 - 117).

Primary Author, with assistance from Dr. Rui Min, Dr. Wen-Ben Jone, and Dr. Yiming Hu.

## UNIVERSITY OF CINCINNATI – MASTERS THESIS REGISTRY

June 2008

“Location Cache Design and Performance Analysis for Chip Multiprocessors” (2008 Edition, Pages 1 - 98).

**AWARDS & HONORS**

## CAPITAL ACCUMULATION PLAN AWARD

February 2011

Stock-based bonus awarded to the Top 5% of engineers in the organization, and personally approved by both the president of the Nova Engineering division and the president of the entire L-3 organization.

## SPIRIT OF EXCELLENCE AWARD

May 2009

Awarded for outstanding effort on the ATDL program, including involvement in a personal demonstration to a General in the US Army.

## WILLIAM L. BADGER AWARD

March 2006

Awarded as part of GE’s nationwide Engineering Recognition Day for development and deployment of the MateCheck engine balancing hardware and software.